AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently amended): A method for filling a uniform mask layer in a trench of a trench capacitor, comprising:

providing a semiconductor substrate, wherein the semiconductor substrate has a dense trench area and a less dense trench area with a plurality of trenches formed in both areas respectively;

forming a mask layer covering the semiconductor substrate, wherein the trenches are filled with the mask layer;

anisotropically etching the mask layer at an angle until the dense trench area and the less dense trench area in the semiconductor substrate are exposed to leave the mask layer in the trenches; and

etching the mask layers in the trenches, and a uniform thickness of the mask layer in each trench is achieved.

Claim 2 (Original): The method for filling a uniform mask layer in a trench of a trench capacitor of claim 1, wherein the angle is greater than 45 degrees relative to the normal angle.

Claim 3 (Original): The method for filling a uniform mask layer in a trench of a trench capacitor of claim 1, wherein the mask layer is a photoresist layer.

Claim 4 (Currently amended): A method for filling a uniform mask layer in a trench of a trench capacitor of a DRAM, comprising:

providing a semiconductor substrate, wherein a first liner layer and a second liner layer sequentially formed thereon, and the semiconductor substrate has a dense trench area and a less dense trench area with a plurality of trenches formed in both areas respectively;

conformably forming a doped insulating layer covering the second liner layer and the trenches;

forming a photoresist layer covering the doped insulating layer and the trenches are filled with the photoresist layer;

anisotropically etching the photoresist layer at an angle until the dense trench area and the less dense trench area in the semiconductor substrate are exposed to leave the photoresist layer in the trenches;

etching the photoresist layers in the trenches, and a uniform thickness of the photoresist layers in each trench is achieved;

etching the doped insulating layer using the photoresist layers as etching masks until the exposed doped insulating layer is removed to leave the doped insulating layer in the trenches;

removing the photoresist layer; and

diffusing the doped insulating layers to form a plurality of doped areas in the semiconductor substrate, wherein the doped areas are substantially the same in size.

Claim 5 (Original): The method for filling a uniform mask layer in a trench of a trench capacitor of claim 4, wherein the first liner layer is a liner oxide layer.

Claim 6 (Previously presented): The method for filling a uniform mask layer in a trench of a trench capacitor of claim 4, wherein the second liner layer is a liner nitride layer.

Claim 7 (Original): The method for filling a uniform mask layer in a trench of a trench capacitor of claim 4, wherein the doped insulating layer is an ASG layer.

Claim 8 (Original): The method for filling a uniform mask layer in a trench of a trench capacitor of claim 4, wherein the angle is greater than 45 degrees relative to the normal angle.

Claim 9 (Currently amended): A method for forming a uniform bottom electrode in a trench of a trench capacitor, comprising:

providing a semiconductor substrate, wherein the semiconductor substrate has a dense trench area and a less dense trench area with a plurality of trenches formed in both areas respectively;

sequentially forming a first liner layer, a second liner layer, a mask layer, and a patterned photoresist layer with a plurality of openings, wherein a portion of the mask layer is exposed via the openings;

sequentially etching the exposed mask layer, the second liner layer, the first liner layer, and the semiconductor substrate using the patterned photoresist layer as an etching mask to form a plurality of trenches in a dense trench area and a less dense trench area;

sequentially removing the patterned photoresist layer and the mask layer;

conformably forming a doped glass layer covering the second liner layer and the trenches;

forming a photoresist layer covering the doped glass layer, and the trenches are filled with the photoresist layer;

anisotropically etching the photoresist layer at an angle until the dense trench area and the less dense trench area in the semiconductor substrate are exposed to leave the photoresist layer in the trenches;

etching the photoresist layer to a predetermined depth in the trenches, and a remaining photoresist layer is formed;

removing the exposed doped glass layer using the remaining photoresist layer as a mask;

removing the remaining photoresist layer;

annealing the semiconductor substrate to form an ion doped area as a bottom electrode in the semiconductor substrate; and

removing the doped glass.

Claim 10 (Original): The method for forming a uniform bottom electrode in a trench of a trench capacitor of claim 9, wherein the first liner layer is a liner oxide layer.

Claim 11 (Previously presented): The method for forming a uniform bottom electrode in a trench of a trench capacitor of claim 9, wherein the second liner layer is a liner nitride layer.

Claim 12 (Original): The method for forming a uniform bottom electrode in a trench of a trench capacitor of claim 9, wherein the mask layer is a BSG layer.

Claim 13 (Original): The method for forming a uniform bottom electrode in a trench of a trench capacitor of claim 9, wherein the doped insulating layer is an ASG layer.

Claim 14 (Original): The method for forming a uniform bottom electrode in a trench of a trench capacitor of claim 10, wherein the angle is greater than 45 degrees relative to the normal angle